AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in this application.

1.(Original) A circuit for re-sampling N data inputs comprising:

a timing error detector sub-circuit having a first input coupled to a symbol rate clock and a second input coupled to a strobe;

~~an~~ a numerically controlled oscillator having an input coupled to an output of the timing error-detector sub-circuit and N timing signal outputs for outputting N timing signals in parallel and a second output for outputting the strobe; and

at least one fractional interpolator having parallel inputs coupled to N data inputs in parallel and to the N timing signals in parallel, for outputting N data outputs in parallel, wherein N is an integer greater than or equal to one.

2.(Original) The circuit of claim 1 wherein the oscillator comprises a plurality of N amplifiers each defining a different gain, and wherein the strobe comprises a most significant bit selected from an output of one of the amplifiers, and wherein N is an integer greater than one.

3.(Original) The circuit of claim 2 wherein each of the N timing signals are coupled to an output of an associated amplifier, and each timing signal except that coupled to a highest gain amplifier is independent of a most significant bit output from said associated amplifier.

4.(Currently Amended) The circuit of claim 1 wherein the fractional interpolator ~~filter~~ comprises:

a shift register having parallel inputs coupled to the N data inputs and to the strobe; and

N ~~error formatters~~bit splitters each having an input coupled to a timing signal, for each outputting a first error value that depends at least in part from a most significant bit (MSB) defined by the timing signal and for outputting a second error value that depends at least in part from at least one other bit defined by the timing signal that is not the MSB.

5.(Original) The circuit of claim 4 wherein the fractional interpolator filter further comprises:

N sub-blocks each having an input coupled to an output of the shift register and an input coupled to an output of an error-formatter.

6.(Original) The circuit of claim 5 wherein the sub-blocks are of the type Farrow sub-blocks, linear interpolators, or polynomial interpolators.

7.(Original) The circuit of claim 1 wherein the error detector sub-circuit operates to synchronize the strobe to a positive edge of the input that is coupled to the symbol rate clock.

8.(Currently Amended) ~~The circuit of claim 7~~ A circuit for re-sampling N data inputs comprising:

a timing error detector sub-circuit having a first input coupled to a symbol rate clock and a second input coupled to a strobe;

an oscillator having an input coupled to an output of the timing error-detector sub-circuit and N timing signal outputs for outputting N timing signals in parallel and a second output for outputting the strobe; and

at least one fractional interpolator having parallel inputs coupled to N data inputs in parallel and to the N timing signals in parallel, for outputting N data outputs in parallel, wherein N is an integer greater than or equal to one

wherein the error detector sub-circuit operates to synchronize the strobe to a positive edge of the input that is coupled to the symbol rate clock and comprises:

a first state machine for generating and outputting a pulse based on the symbol rate clock;

a second and a third state machine in electrical parallel with one another, each having an input coupled to the strobe and to an output of the first state machine; and

wherein the oscillator input is coupled to an output of at least one of the second or third state machines.

9.(Original) The circuit of claim 8 wherein the error detector sub-circuit further comprises a loop filter defining a gain determined by a microprocessor, wherein the oscillator input is coupled to an output of the loop filter.

10.(Original) The circuit of claim 7 wherein the error detector sub-circuit synchronizes the strobe by adjusting a period between two consecutive strobes to match a period defined by the symbol rate clock.

11.(Original) The circuit of claim 7 wherein the error detector sub-circuit further comprises an oscillator data clock having an input coupled to the strobe, and an integrator having a first input coupled to an output of the oscillator data clock and a second input coupled to an output of the symbol rate clock, the integrator having an output coupled to an inverter, and wherein the oscillator input is coupled to an output of the inverter.

12.(Original) The circuit of claim 1 wherein N is greater than one, and the N data outputs are output at a rate at least equal to a symbol rate determined by the symbol rate clock.

13.(Currently Amended) A method for re-sampling ~~a~~ parallel data samples ~~input at any fractional time~~ within of a symbol period, comprising:

synchronizing a local clock to a symbol clock;

determining a plurality of N parallel timing signals based on the synchronized local clock;

providing the N parallel timing signals and a strobe from the local clock to an interpolating filter;

re-sampling each of a plurality of N data sample inputs at a time within a symbol period determined by individual ones of the plurality of N timing signals and the strobe; and

providing a timing feedback to synchronize the local clock to the symbol clock.

14.(Original) The method of claim 13 wherein synchronizing a local clock to a symbol clock comprises determining a difference between the symbol rate clock signal and one of at least two data strobes and providing a frequency adjustment output based on the difference.

15.(Original) The method of claim 13 wherein the timing feedback comprises a most significant bit of an amplified frequency signal accumulated in a register.

16.(Canceled)

17.(Currently Amended) A method for fractionally re-sampling a data sample, comprising:

inputting a symbol rate and a data strobe;

measuring a difference between the data strobe and the symbol rate;

adjusting a next data strobe to match the symbol rate;

determining a plurality of N parallel timing signals based on the difference; and

fractionally re-sampling in parallel a plurality of N data samples at a time within a symbol period defined by individual ones of the plurality of N timing signals.

18.(Currently Amended) A circuit for re-sampling ~~a data sample input~~ a plurality of N data sample inputs in parallel comprising:

a detector loop having an input coupled to an output of a symbol rate clock signal and to a data strobe, for determining a difference therebetween, and for providing a frequency adjustment output based on said difference;

a numerically controlled oscillator NCO having an input coupled to the frequency adjustment output, and for outputting the data strobe and a plurality of N timing signals in parallel; and

a fractional interpolator having ~~an~~ a plurality of N parallel data inputs coupled to ~~a~~ N data sample inputs, a first timing input coupled to the data strobe, and a plurality of N second timing inputs coupled to individual ones of the N timing signals, for re-sampling in parallel the N data sample inputs at a time within a symbol period defined by the individual ones of the timing signals.

19.(Canceled)

20.(Currently Amended) A circuit for interpolating a plurality of data points from a plurality of data samples comprising:

means for separating a plurality of at least 2N input data samples into N parallel input streams, the 2N data samples defining a sample rate of $1/T_S$;

a fractional interpolator having an input coupled to each of the N parallel input streams for interpolating in parallel at least one interpolated data point from the data samples input along each of the N input streams, and N parallel outputs for outputting in parallel the interpolated data points; and

a numerically controlled oscillator NCO having ~~an~~ a plurality of N outputs coupled to ~~an~~ respective N inputs of the fractional interpolator for providing N timing signals for ~~each~~ respective ones of the interpolated data points;

wherein the interpolated data points exhibit an output rate of 1/T that is cyclically independent of the sample rate $1/T_s$.

21.(Original) The circuit of claim 20 wherein the NCO has an input coupled to an output of a timing source that is independent of a timing source used for the input data samples.